Panagiotis-Taxiarchis Giannakoy

Curriculum Vitae

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As an ambitious and hard-working person, I am highly motivated by challenges in technological advancements. I am fulfilling multiple tasks in every-day basis, effectively working under pressure. Have worked successfuly as a part of a team and alone, opting for discussing and providing well thougt out solutions and ideas. I would wellcome the oportunity to discuss my suitability in more detail.

Education

2012–2015 (estimated) **Master in Computer Science**, *University of Thessaly*, Volos.
Currently developing master thesis (final)

2006–2012 **Bachelor in Computer Science**, *University of Thessaly*, Volos, *7.52/10*.
Specialized in Hardware and Computer Architecture

Master Thesis

Title *Dynamic Noise Margin Analysis in SRAM Cells*

Supervisors Professor George Stamoulis, Assistant Professor Nestor Eumorfopoulos & Assistant Professor Panagiota Tsompanopoulou

Description (In progress) This thesis proposes an analytical model for dynamic stability analysis of a typical 6T SRAM cell under device mismatch. Implementation and verification of the proposed model.

Bachelor Thesis

Title *Timing analysis of digital circuits using technologies under 45nm*

Supervisors Professor George Stamoulis & Assistant Professor Nestor Eumorfopoulos

Description Development of a source to source transformation tool for converting HDL netlists to SPICE netlists with the ability of variating transistor level parameters.
Analysis of the effect of the transistor width variation on the timing characteristics of a digital circuit using Monte Carlo techniques for the production of variation samples.

Experience

Vocational

2014–Present **Research Assistant**, Institute for Research & Technology Thessaly, Volos, Greece.
Nanotrim–Continuous Transistor Sizing Toolset for nanoscale IC optimization
- Design of the layout manipulation automation.
- Design and implementation of GDS2trim layout manipulation utility

2015–Present **Developer**, *Electronics Lab, University of Thessaly*, Volos, Greece.
EcoSystem - Intelligent system for programming and managing building autmation Hardware platform configuration & porting of Ubuntu Linux on AVNet Microzed embedded platform.

2012–2015 **Teaching Assistant**, *ECE dept., University of Thessaly*, Volos, Greece.
Courses:
- Digital Electronics
- Digital Design
- Electrical Drawing

July 2010 – August 2010 **Summer Intern**, *Nanotropic*, Athens, Greece.
Transistor level timing analysis of digital circuits

Awards

2014 Honorable Mention – TAU Timing Analysis Contest, TAU workshop 2014

Projects

Common Path Pessimism Removal Algorithm for TAU contest 2014.
Timing analysis tool for the TAU 2014 contest. The main feature is the removal of unnecessary but inherent pessimism during timing analysis in the presence of variation.(Common path pessimism-removal taiming analysis tool)

SPICE - type Circuit Simulator.
Design and implementation of SPICE - like circuit simulation software. Features implemented: dc, sweep, transient, and variable timestep transient analysis.

Memory Hierarchy Simulator, semester project, Computer Architecture course.
Software implementation of a memory hierarchy simulator of a typical processing unit. The implementation features L1, L2, and L3 cache simulation along with a virtual to physical page translation mechanism.

AVS video decoder port to FPGA, semester project, Embedded Systems course.
Experimental Evaluation of the performance of the AVS video decoder on FPGA platform, using embedded Linux OS on microblaze processor.

Power Grid Analysis & Optimization with geometric programming, semester project, Microprocessor Design course.
Power distribution modeling, and transistor width determination for clock frequency, power consumption and area optimization using geometric programming methods.

Business Plan Implementation, semester project, Enterpreneurship Course.
Development of a full business plan for utilizing the RFID technology on the field of care of sensitive population groups (children/elderly people).

Publications

2015 Author, "GDS2trim: Physical Layout Manipulation Utility for continuous transistor sizing", 2015 *4th International conference on Modern Circuits and System Technologies*

2015 Co-author, "CCSOpt: A Continuous Gate-Level Resizing Tool", 2015 *4th International conference on Modern Circuits and System Technologies*

2014 Co-author, "TKtimer: Fast & Accurate Clock Network Pessimism Removal",*2014 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*

Technical skills

Operating Systems: SunOS, Linux (RedHat/ Debian variants), Windows

Programming Languages:
Advanced: C
Very Good: C++, PYTHON, MATLAB
Basic: Java, Perl, Tcl, CUDA, Verilog

CAD Tools: Cadence RTL Compiler(Basic), Cadence SoC Encounter(Basic Flow), Synopsys Design Compiler, Synopsys Nanotime, Synopsys HSPICE (analyses for digital circuits), Xilinx Vivado(Basic Flow)

Other: Eclipse, Xilinx SDK, Petalinux SDK, Microsoft Visual Studio, Microsoft Office, Matlab, Latex, Git

General:
- Knowledge of the ASIC design flow and the corresponding tools for each stage.
- Knowledge of algorithms used in EDA:
  - Brief: Placement, Routing
  - Detailed: Logical synthesis, Timing Analysis, Circuit Simulation
- Embedded design flow / Embedded Development (Full OS integration)

Communication Skills

2015 Oral Presentation at the 4th International conference on Modern Circuits and System Technologies

2014 Oral Presentation at the 2014 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)

Languages

Greek **Mothertongue**

English **Proficient** *near native / fluent*

German **Basic** *basic communication skills / working knowledge*

Interests

- Music
- Dancing
- Martial Arts
- Traveling