Garyfallou Dimitrios

Curriculum Vitae, Updated: 1st of May 2017

Contact Information

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Personal Information

- Date of birth: May 22th 1991
- Place of birth: Thessaloniki, Greece
- Greek Nationality and Citizenship

Experience

- **Researcher at University of Thessaly**
  October 2015 – Today
- **Researcher at Electronics Lab**
  University of Thessaly
  March 2014 – Today
- **Researcher at Centre for Research & Technology HELLAS**
  June 2015 – October 2015

Education

- November 2015 – Today:
  PhD. student in Electrical and Computer Engineering Department,
  University of Thessaly, Volos, Greece
- September 2014 – November 2015:
  Master in "Science and Technology of Electrical and Computer Engineering",
  University of Thessaly, Volos, Greece
  G.P.A: 9.79/10
- September 2009 – September 2014 :
  Diploma in Electrical and Computer Engineering Department,
  University of Thessaly, Volos, Greece
  G.P.A: 7.40/10
- June 2013 – August 2013:
  Intern at "RAM COMPUTER",
  Thessaloniki, Greece

Foreign Languages

- **English**, CCE(Certificate of Competency in English), University of Michigan
- **French**, DELF(Diplôme d'études en langue française) B2

Honors and Awards

- PhD Studies Fellowship : June 2016 - June 2017
- Beneficiary of ECE Department Master Studies Fellowship (based on ranking) : September 2014 - November 2015

Areas of Interest

- EDA / CAD Tools
- High Performance Computing

Technical Skills

- **Programming Languages**:
  C, C++, Python, Java, NesC, Mips Assembly
- **Hardware Description Languages:**
  Verilog
- **Parallel Programming Languages and Libraries**:
  CUDA, OpenMP, Message Passing Interface (MPI), POSIX Threads
- **Mathematics Software:**
  MathWorks® Matlab
- **Performance Profilers:**
  Intel VTune Performance Analyzer, NVIDIA® Visual Profiler
- **Hardware CAD Tools:**
  Xilinx Vivado Design Suite, Synopsys PrimeTime, Mentor Graphics QuestaSim
- **Operating Systems**:
  Debian/Fedora based Linux, Windows, TinyOS
- **Other know-how**:
  Eclipse, NVIDIA® Nsight Eclipse Edition, TOSSIM Simulator, Microsoft Office, Revision control system (Git), Scrapy Framework, Vim, Joomla, LATEX Typesetting

Funded Projects

- **NanoTrim: A Continuous Transistor Re-sizing Toolset.**
  - **Co-Funded by**: European & National Funds
  - **Partners:** CERTH/IRETETH, UTH, AUTH, HELIC S.A, NESSOS S.A
  - **Duties**:
    Software design and development

- **ECOSYSTEM: An FPGA based smart home system.**
  - **Partners:** UTH, CONVERGE S.A
  - **Duties**:
    Software design and development

Journal Publications

- Antonios N. Dadaliaris, Panagiotis Oikonomou, Maria G. Koziri, Evangelia Nerantzaki, Yannis Hatzaras, Dimitrios Garyfallou, Thanasis Loukopoulos, Georgios I. Stamoulis. '**Heuristics to Augment the Performance of Tetris Legalization: Making a Fast but Inferior Method Competitive**'. Accepted for publication in *Journal Of Low Power Electronics*, Vol. 13, N° 2, June 2017, *American Scientific Publishers*

Diploma Thesis

- April 2014 – September 2014
  Title: **«Simulation of large-scale circuits with Steiner node preconditioners on parallel architectures»**

  The solution of linear systems in the form Ax = b, on Symmetric Diagonal Dominant matrices (SDDs) is a problem of fundamental theoretical importance but also one with a myriad of applications in numerical mathematics, engineering and science. In this diploma thesis, I implemented and accelerated an SDD solver based on graph theory and Steiner preconditioners. The development was based on the OpenMP library while the runtime hotspots of the algorithm were mapped to an NVIDIA Tesla C2075 GPU using the CUDA programming model.

  Advisors: Nestoras Eumorfopoulos, Christos D. Antonopoulos

Master Thesis

- April 2015 – September 2015
  Title: «**Development and Optimization of a combinatorial multigrid algorithm for large scale circuit simulation on massively parallel architectures**»

  The simulation of very large scale circuits leads to the solution of very large sparse SDD systems. The purpose of this master thesis was the acceleration of a linear SDD graph based solver for linear systems that arise in circuit simulation. This thesis was based on my diploma thesis and achieved a runtime acceleration up to 10x over the sequential implementation, taking the advantage of the great runtime improvements that a massively parallel architecture (GPU) can offer.

  Advisors: Nestoras Eumorfopoulos, George Stamoulis, Panagiota Tsompanopoulou

PhD

Thesis

- November 2015 – Today
  Title: «**VLSI Circuit Design and Optimization Under Voltage Drop Constraints Derived From an EVT Framework**»

  VLSI designers go after timing and power problems induced by an obsolete methodology instead of the real design issues of the circuit. Gates are oversized to meet overly constrained power supply budgets and unrealistic operating points. In my PhD, I propose a new design and optimization method of the digital circuit that takes into account the IR-drop as it should be, with the aim of implementing faster and lower power circuits. Estimation of the currents drawn by each individual block will be obtained taking into account the effect of the power supply bus, using Extreme Value Theory (EVT) to find a tight upper bound of the worst power current. The gates within the blocks will be resized according to the new worst-case IR-drops, which leads to improved timing, less power, and better designer time utilization. I have already developed an event-driven (DTA) simulator which is based on the NLDM/NLPM and CCS timing/power industrial models. Currently, I work on the IR-drop estimation methodology.

  Advisors: Nestoras Eumorfopoulos, George Stamoulis, Fotis Plessas

Projects*

- **Design and implementation of a Static Timing Analysis tool developed in C/C++ for TAU 2015 timing contest.**

  - *Development of a Verilog and SPEF Parser for TAU 2015 and ISCAS Circuits '89 Benchmarks and of a Liberty Parser for Nangate 45 nm Open Cell Library.*
  - *Setup/Hold Analysis:*
    - *Delay, arrival time, required arrival time and slack calculation.*
  - *Support for any incremental change on the design.*

- **Software implementation of a CAD tool for DC and Transient analysis of Integrated Circuits developed in C language. Term project for CE530 “Circuit Simulation Algorithms”.**

  This project is capable of making both DC and Transient analysis. For the solution of the system that arises for the Very Large Scale Integrated circuits, the user can decide between Direct and Iterative solution methods. The tool can handle both dense and sparse systems using the corresponding optimized data structures.

- **Implementation and Acceleration of the Receiver's Physical Layer Base Band processing on an LTE SDR (Software Defined Radio). Term project for CE435 "Embedded Systems".**

  The aim of this project was to map and accelerate a simulator developed in MATLAB, on a Zynq FPGA. The processing modules were implemented in C language and accelerated using the ARM Cortex-A9 processor. The most time consuming and parallelizable processing steps (FTT, Viterbi Decoder), were implemented and further accelerated as hardware modules.

- **Development of a Virtual Machine and a Middleware for an execution platform running on Wireless Sensor Networks. Term project for CE520 "Wireless Sensor Networks programming".**

  This middleware supports dynamic application installation and uninstallation, parallel execution and communication between applications installed on wireless sensors. The project was developed on the TinyOS operating system using the NesC programming language. This virtual machine was demonstrated on Crossbow imote2 wireless nodes.

- **Implementation of some extra algorithms on a Linux OS using C programming language. Term project for CE321 "Operating Systems".**

  - *Implementation and support for SJF (Shortest Job First) process scheduling policy.*
  - *Activation and modification of the SLOB (Simple List Of Blocks) memory allocator.*
  - *Implementation of the C-LOOK I/O scheduling algorithm.*

- **Software implementation of a FORTRAN320 compiler using C. Term project for CE320 "Compilers".**

  This tool includes the syntax and semantic analysis for a variant of FORTRAN programming language. The syntax analyzer was developed using the Flex tool and the semantic analyzer using the Bison tool.

- **Development of an action game using the OpenGL library. Term project for CE120 "Programming 1".**

  The purpose of this project was the software implementation of a user-interactive game in C programming language using the OpenGL library to create the graphics.

* A complete list of all my projects can be sent after request.

Teaching Experience

- March `16 - June`17
  Teaching Assistant at the undergraduate course «Low Power Design»

  Duties:
  Student assistance / Project and exam evaluation
  Instructor:
  George Stamoulis

- September`15 - March `16
  Teaching Assistant at the undergraduate course «Digital Design»

  Duties:
  Student assistance / Exams evaluation
  Instructor:
  George Stamoulis

- February `15 - September`15
  Teaching Assistant at the undergraduate course «Introduction in electric draw and electrotechnical materials»

  Duties:
  Student assistance / Exams evaluation
  Instructor:
  George Stamoulis

- September `14 - February `15 / September `16 - February `17
  Teaching Assistant at the postgraduate course «Circuit Simulation Algorithms»

  Duties:
  Student assistance / Project and exam evaluation
  Instructor:
  Nestoras Eumorfopoulos

- February `13 - June `13
  Teaching Assistant at the undergraduate course «Theory of computation»

  Duties:
  Student assistance / Evaluation of the term project
  Instructor:
  Manolis Vavalis

Recommendation Letters

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georges@inf.uth.gr
mav@inf.uth.gr